UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/705,996	11/03/2000	Yang Zhao	MEMSC-001XX	6364

207 7590 03/08/2004

WEINGARTEN, SCHURGIN, GAGNEBIN & LEBOVICI LLP
TEN POST OFFICE SQUARE
BOSTON, MA 02109

EXAMINER	
SHECHTMAN, SEAN P	
ART UNIT	**PAPER NUMBER**
2125	5

DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/705,996	Applicant(s) ZHAO ET AL.	
	Examiner Sean P. Shechtman	Art Unit 2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8-15,20,21 and 23-25* is/are rejected.

7)☒ Claim(s) *2-7,16-19 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-25 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 23 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 23 and 24 recite the limitation "the chip" in lines 3 and 2 respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter referred to as AAPA) in view of U.S. Pat. No. 4,595,884 to Miller.

Referring to claim 15, AAPA teaches a method for operating a convective acceleration sensor, the acceleration sensor including a heater element and a plurality of temperature sensing elements, the method comprising the steps of:

generating a differential output voltage indicative of a magnitude of acceleration applied along at least one axis passing through the heater element and the plurality of temperature sensing elements (See page 1, line 15 – page 2, line 20 of the instant specification);

AAPA fails to teach the method above, further comprising: generating a common-mode output voltage corresponding to the differential output voltage; generating a control output proportional to the common mode output voltage; and regulating the common-mode output voltage using the control output.

However, Miller teaches a method/instrumentation amplifier that generally relates to transducer amplifiers (Abstract; Col. 1, lines 6-10; Col. 2, lines 42-46; Col. 5, lines 20-24Col. 8, lines 26-30 of '884),

Wherein, a bridge circuit (i.e., transducer) produces a differential voltage signal and generates a common-mode output voltage corresponding to the differential output voltage (Col. 8, lines 49-62; Col. 5, lines 49-51 of '884);

generating a control output proportional to the common mode output voltage (Col. 5, lines 54-66 of '884); and

regulating the common-mode output voltage using the control output (Col. 5, lines 54-66 of '884).

Examiner respectfully asserts that the error component multiplied by the gain to be superimposed on the common-mode signal to attenuate the common-mode signal is a control output proportional to the common mode voltage. Furthermore, examiner respectfully asserts

that attenuation is a form of regulation, and therefore the common-mode voltage is regulated by the control signal.

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to combine the teachings of Miller with AAPA.

One of ordinary skill in the art would have been motivated to combine these references because Miller teaches a transducer amplifier that has a high common mode rejection with lower current drain. Furthermore, Miller teaches a less expensive transducer amplifier that has a high common mode rejection (Col. 1, lines 6-9 of '884). Further still, Miller provides for an improved transducer amplifier with a lower input offset voltage drift (Abstract, last couple lines of '884).

4. Claims 1, 8-11, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,945,601 to Hosoi in view of "A Three-Axis Micromachined Accelerometer with a CMOS Position-Sense Interface and Digital Offset-Trim Electronics" by Lemkin.

Referring to claims 1 and 15, Hosoi teaches an integrated convective accelerometer chip and control thereof (Abstract; Fig. 21), comprising:

a convective acceleration sensor including a heater element and a plurality of temperature sensing elements (Figs. 1-6), the plurality of temperature sensing elements being operative to generate a differential output voltage indicative of a magnitude of acceleration applied along at least one axis passing through the heater element and the plurality of temperature sensing elements (Figs. 1-6);

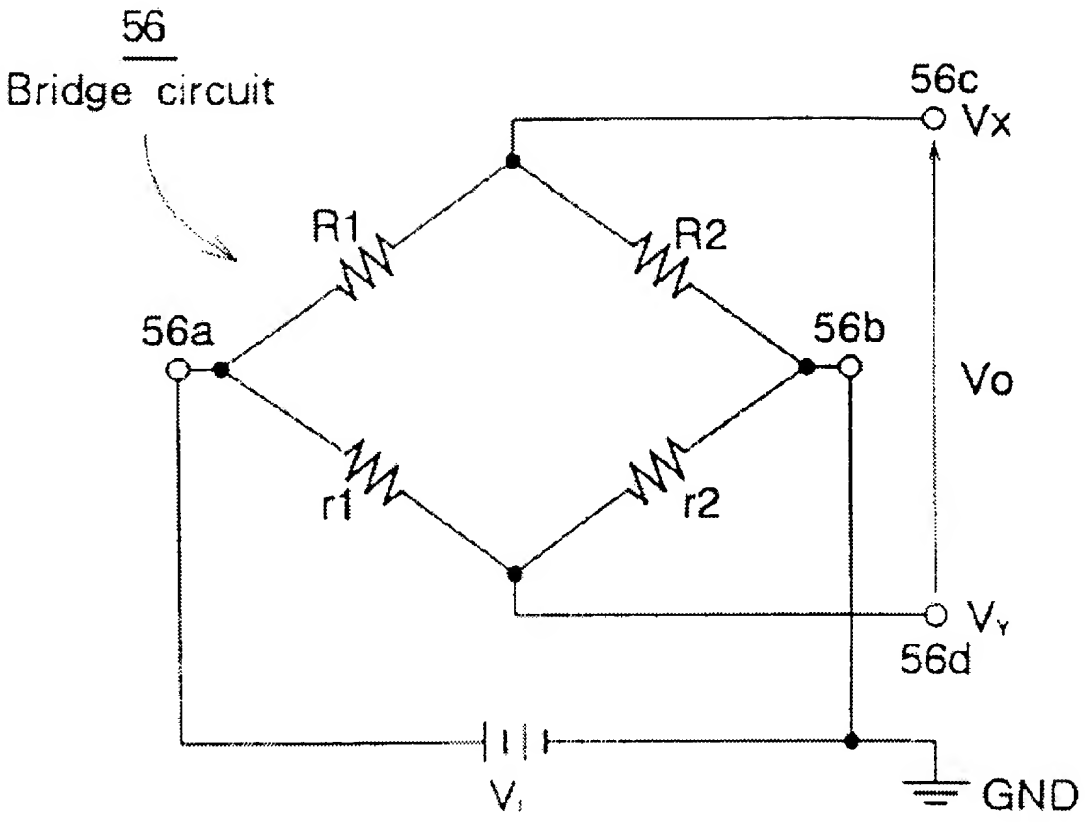
Referring to claim 8, Hosoi teaches the chip above, further including a reference voltage generator operative to generate a reference voltage level (Fig. 5, element 17, Col. 5, line 57 – Col. 6, line 14).

Referring to claim 9, Hosoi teaches the chip above, wherein the reference voltage level is a fixed voltage level (Fig. 5, element 17, conventional circuit element for a constant voltage source).

Referring to claim 10, Hosoi teaches the chip above, wherein the reference voltage level is proportional to a supply voltage level (Fig. 5, element 17).

Referring to claim 11, Hosoi teaches the chip above, wherein each temperature sensing element has a respective first terminal and a respective second terminal, wherein the respective second terminals of the temperature sensing elements are connected, wherein the acceleration sensor is operative to generate the differential output voltage across the respective first terminals of the temperature sensing elements (Figs. 5 and 16), and wherein the acceleration sensor is further operative to set the connected respective second terminals of the temperature sensing elements to a desired voltage level proportional to the reference voltage level (See Figs. 5 or 16, elements 56a and 56b).

Fig. 16



Referring to claim 13, Hosoi teaches the chip above, wherein acceleration sensor including the heater element and the plurality of temperature sensing elements are silicon micro-machined devices (Abstract; Fig. 21).

Referring to claims 1 and 15, Hosoi fails to teach amplification circuitry operative to generate a corresponding common-mode output voltage; and control circuitry configured to receive the common-mode output voltage generated by the amplification circuitry and operative

to generate a control output proportional thereto, the control circuitry being further operative to regulate the common-mode output voltage using the control output.

However, referring to claims 1 and 15, Lemkin teaches an integrated accelerometer chip with mechanical sensors (See Page 456, Abstract, lines 1-3; Page 465, Fig. 13; Page 467, Section X) that can be "integrated with CMOS for monolithic sensor based systems" (See Page 456, left column, 3rd paragraph) and control thereof, wherein reference is made to a broad range of compatible sensor-based systems (See the references section of page 467, references 1 and 2) defined as those systems that can be "integrated with CMOS for monolithic sensor based systems" (See again, page 456, 3rd paragraph), the chip and control thereof comprising:

An acceleration sensor being operative to generate a differential output voltage indicative of a magnitude of acceleration applied along at least one axis passing through the sensing elements (See page 456, Fig. 1; See page 457, section II, right column, a "differential sensor interface"; Page 458, Fig. 4).

amplification circuitry configured to receive the differential output voltage generated by the sensing elements and operative to generate a corresponding common-mode output voltage (Page 458, left column, 1st paragraph); and

control circuitry configured to receive the common-mode output voltage generated by the amplification circuitry and operative to generate a control output proportional thereto, the control circuitry being further operative to regulate the common-mode output voltage using the control output (Page 458, right column, 2nd paragraph – end of column; See Page 459, Fig. 5; Page 460, Fig. 6).

Lemkin teaches a differential sensor interface, wherein deltaVicm is the difference in the input common mode voltage in response to the voltage step (Page 458, left column). Lemkins teachings are specifically directed towards solving the problems associated with the input common-mode voltage shift causing offsets errors and placing severe requirements on the op-amp (See Page 458, left column, last 2 paragraphs; See also page 458, right column).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to combine the integrated accelerometer chip with common-mode control of Lemkin with the integrated convective accelerometer chip of Hosoi.

One of ordinary skill in the art would have been motivated to combine these references because Lemkin teaches an accelerometer with digital output that has been realized on a single chip (See page 467, Section X). Furthermore, Lemkin teaches techniques used in a differential interface that attenuate many sources of error including op-amp offset, op-amp flicker noise, charge rejection, and sampling noise. Further still, Lemkin teaches a mechanical sense element driven by sense-voltage pulses, enabling differential circuitry to be used throughout the sense interface (See page 467, Section X). Further still, Lemkin teaches solving the problems associated with the input common-mode voltage shift causing offsets errors and placing severe requirements on the op-amp (See Page 458, left column, last 2 paragraphs; See also page 458, right column).

Further still, the recitation of "an integrated convective accelerometer chip" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for

completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

5. Claims 1, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,182,509 to Leung in view of "A Three-Axis Micromachined Accelerometer with a CMOS Position-Sense Interface and Digital Offset-Trim Electronics" by Lemkin.

Referring to claims 1 and 15, Leung teaches an integrated convective accelerometer chip and control thereof (Col. 2, lines 11-43), comprising:

a convective acceleration sensor including a heater element and a plurality of temperature sensing elements (Abstract; Fig. 11), the plurality of temperature sensing elements being operative to generate a differential output voltage indicative of a magnitude of acceleration applied along at least one axis passing through the heater element and the plurality of temperature sensing elements (Col. 2, lines 29-30; Col. 9, claims 9 and 16; Col. 5, lines 13-27); Leung clearly teaches amplification circuitry configured to receive the differential output voltage generated by the plurality of temperature sensing elements (See Fig. 11 below).

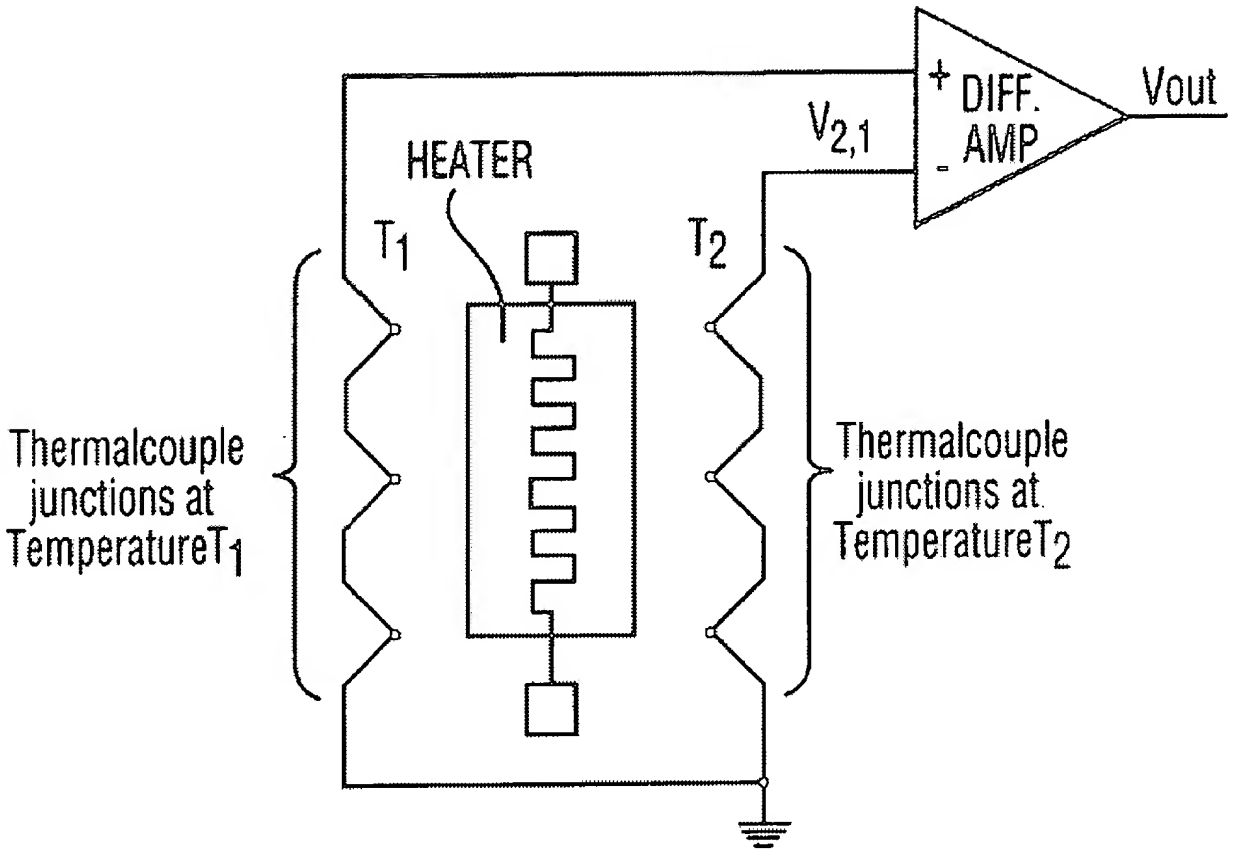


FIG. 11

Referring to claim 13, Leung teaches the chip above, wherein acceleration sensor including the heater element and the plurality of temperature sensing elements are silicon micro-machined devices (Col. 4, lines 21-22; Col. 8, lines 27-31; Col. 9, claim 11).

Referring to claims 1 and 15, Leung fails to teach amplification circuitry operative to generate a corresponding common-mode output voltage; and control circuitry configured to receive the common-mode output voltage generated by the amplification circuitry and operative

to generate a control output proportional thereto, the control circuitry being further operative to regulate the common-mode output voltage using the control output.

However, referring to claims 1 and 15, Lemkin teaches an integrated accelerometer chip with mechanical sensors (See Page 456, Abstract, lines 1-3; Page 465, Fig. 13; Page 467, Section X) that can be "integrated with CMOS for monolithic sensor based systems" (See Page 456, left column, 3rd paragraph) and control thereof, wherein reference is made to a broad range of compatible sensor-based systems (See the references section of page 467, references 1 and 2) defined as those systems that can be "integrated with CMOS for monolithic sensor based systems" (See again, page 456, 3rd paragraph), the chip and control thereof comprising:

An acceleration sensor being operative to generate a differential output voltage indicative of a magnitude of acceleration applied along at least one axis passing through the sensing elements (See page 456, Fig. 1; See page 457, section II, right column, a "differential sensor interface"; Page 458, Fig. 4).

amplification circuitry configured to receive the differential output voltage generated by the sensing elements and operative to generate a corresponding common-mode output voltage (Page 458, left column, 1st paragraph); and

control circuitry configured to receive the common-mode output voltage generated by the amplification circuitry and operative to generate a control output proportional thereto, the control circuitry being further operative to regulate the common-mode output voltage using the control output (Page 458, right column, 2nd paragraph – end of column; See Page 459, Fig. 5; Page 460, Fig. 6).

Lemkin teaches a differential sensor interface, wherein deltaVicm is the difference in the input common mode voltage in response to the voltage step (Page 458, left column). Lemkins teachings are specifically directed towards solving the problems associated with the input common-mode voltage shift causing offsets errors and placing severe requirements on the op-amp (See Page 458, left column, last 2 paragraphs; See also page 458, right column).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to combine the integrated accelerometer chip with common-mode control of Lemkin with the integrated convective accelerometer chip of Leung.

One of ordinary skill in the art would have been motivated to combine these references because Lemkin teaches an accelerometer with digital output that has been realized on a single chip (See page 467, Section X). Furthermore, Lemkin teaches techniques used in a differential interface that attenuate many sources of error including op-amp offset, op-amp flicker noise, charge rejection, and sampling noise. Further still, Lemkin teaches a mechanical sense element driven by sense-voltage pulses, enabling differential circuitry to be used throughout the sense interface (See page 467, Section X). Further still, Lemkin teaches solving the problems associated with the input common-mode voltage shift causing offsets errors and placing severe requirements on the op-amp (See Page 458, left column, last 2 paragraphs; See also page 458, right column).

Furthermore, examiner respectfully notes that the technology of Leung provides for a sensor-based system that are integrated with CMOS for monolithic sensor based silicon substrates (Col. 8, lines 27-31; Col. 9, claim 11) and Lemkin defines the sensor-based systems compatible with the accelerometer chip as a broad range of sensor-based systems (See the

references section of page 467, references 1 and 2) that can be "integrated with CMOS for monolithic sensor based systems" (See again, page 456, 3rd paragraph).

Further still, the recitation of "an integrated convective accelerometer chip" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

6. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,182,509 to Leung in view of "A Three-Axis Micromachined Accelerometer with a CMOS Position-Sense Interface and Digital Offset-Trim Electronics" by Lemkin as applied to claims 1 and 15 above, and further in view of U.S. Pat. No. 5,339,285 to Straw.

Referring to claim 21, Leung teaches the method above, further including the steps of converting the differential output voltage to a single-ended output voltage indicative of the magnitude of acceleration applied along the at least one axis (Col. 4, lines 46-57; Col. 5, lines 13-27 of '285).

Leung fails to teach setting the single-ended output voltage to provide a desired level of gain.

However, referring to claim 21, Straw teaches analogous art, wherein an integrated circuit (Col. 1, lines 21-23; Col. 1, lines 24-60 of '285) to be used with an accelerometer includes the steps of converting the differential output voltage to a single-ended output voltage indicative of the magnitude of acceleration and setting the single-ended output voltage to provide a desired level of gain (Col. 2, lines 12-35; Col. 3, lines 27-29; Col. 4, lines 49-51 of '285).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to combine the integrated chip gain control of Straw with the integrated convective accelerometer chip of Leung.

One of ordinary skill in the art would have been motivated to combine these references because Straw teaches an improved preamplifier in a single monolithic integrated circuit in small size without the need for any external components. Furthermore, the preamplifier uses low power and has a wide bandwidth and is suitable for adjustable gain and corner frequency. Furthermore, the integrated circuit is insensitive to hydrostatic pressure and silicon substrate noise. Further still, Straw teaches a differential to single ended converter with good common-mode rejection ratio (Col. 1, line 63 – Col. 2, line 35 '285).

7. Claims 8, 10, 12, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,182,509 to Leung in view of "A Three-Axis Micromachined Accelerometer with a CMOS Position-Sense Interface and Digital Offset-Trim Electronics" by Lemkin as applied to claims 1 and 15 above, and further in view of U.S. Pat. No. 5,229,709 to Pfennings. Claims 12, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,945,601 to Hosoi in view of "A Three-Axis Micromachined Accelerometer with a CMOS

Position-Sense Interface and Digital Offset-Trim Electronics" by Lemkin, as applied to claims 1, 8, and 15 above, and further in view of U.S. Pat. No. 5,229,709 to Pfennings.

Hosoi teaches the chip above, further including the step of temperature compensating the chip (Figs. 10-12; Cols. 9-10 of '601).

Referring to claim 8, Leung fails to teach the chip above, further including a reference voltage generator operative to generate a reference voltage level.

Referring to claim 10, Leung fails to teach the chip above, wherein the reference voltage level is proportional to a supply voltage level.

Referring to claims 12 and 23, Leung and Hosoi fail to teach the chip above, wherein the reference voltage generator is further operative to generate a level proportional to the absolute temperature of the chip.

Referring to claim 24, Leung and Hosoi fail to teach the chip above, further including the step of temperature compensating the chip using the level proportional to the absolute temperature.

However, Pfennings teaches analogous art, wherein a temperature sensing integrated circuit (Title of '709) comprises:

Referring to claim 8, Pfennings teaches a reference voltage generator operative to generate a reference voltage level (Col. 3, lines 39-50 of '709).

Referring to claim 10, Pfennings teaches the chip above, wherein the reference voltage level is proportional to a supply voltage level (Col. 3, lines 47-50 of '709).

Referring to claims 12 and 23, Pfennings teaches the chip above, wherein the reference voltage generator is further operative to generate a level proportional to the absolute temperature of the chip (Col. 3, lines 39-50 of '709).

Referring to claim 24, Pfennings teaches the chip above further including the step of temperature compensating the chip using the level proportional to the absolute temperature (Abstract; Col. 4, lines 45-48 of '709).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to combine teachings of Pfennings with Leung or Hosoi.

One of ordinary skill in the art would have been motivated to combine these references because Pfennings teaches an integrated circuit whose mode of operation is less temperature dependant. Furthermore, Pfennings teaches an integrated circuit wherein the effects of increasing temperature and increasing supply voltage provide a substantially constant switching rates and hot carrier stresses, and therefore, substantially cancel each other out while advantageously intensifying each other at a negative temperature coefficient (Col. 1, lines 46-68 of '709).

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,182,509 to Leung in view of "A Three-Axis Micromachined Accelerometer with a CMOS Position-Sense Interface and Digital Offset-Trim Electronics" by Lemkin as applied to claims 1 and 15 above, and further in view of U.S. Pat. No. 6,683,358 to Ishida. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,945,601 to Hosoi in view of "A Three-Axis Micromachined Accelerometer with a CMOS Position-Sense Interface and

Digital Offset-Trim Electronics" by Lemkin, as applied to claims 1, 8, and 15 above, and further in view of U.S. Pat. No. 6,683,358 to Ishida.

Referring to claim 20, both Leung and Hosoi fail to teach the method above, wherein the second generating step includes the substep of setting the common-mode output voltage to a desired level.

However, referring to claim 20, Ishida teaches analogous art (Col. 1, lines 5-12; Col. 2, lines 58-62 of '358), wherein the step of generating a common-mode output voltage using differential amplifier circuits (Col. 15, line 64 – Col. 16, line 4 of '358) includes the substep of setting the common-mode output voltage to a desired level (Fig. 8; Col. 8, lines 7-15 of '358).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to combine teachings of Ishida with Leung or Hosoi.

One of ordinary skill in the art would have been motivated to combine these references because Ishida teaches a silicon integrated accelerometer that has an inexpensive sensor body and has a simplified circuit configuration and is capable of removing the effects of the offset outputs regardless of imbalance in fabrication conditions. Furthermore, Ishida provides improved measurement accuracy by suppressing sensitivities to off-axis as well as by improving the detection sensitivities to the sensitive axis (Col. 3, lines 56-65 of '358).

9. Claims 14 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,182,509 to Leung in view of "A Three-Axis Micromachined Accelerometer with a CMOS Position-Sense Interface and Digital Offset-Trim Electronics" by Lemkin as applied to claims 1 and 15 above, and further in view of AAPA or U.S. Pat. No. 5,861,775 to Chen. Claim

20 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,945,601 to Hosoi in view of "A Three-Axis Micromachined Accelerometer with a CMOS Position-Sense Interface and Digital Offset-Trim Electronics" by Lemkin, as applied to claims 1 and 15 above, and further in view of AAPA or U.S. Pat. No. 5,861,775 to Chen.

Referring to claims 14 and 25, Leung and Hosoi fail to teach the method above, wherein the common-mode output voltage is proportional to power dissipated in the heater element of the convective acceleration sensor.

However, referring to claims 14 and 25, AAPA teaches analogous art, wherein the common-mode output voltage is proportional to power dissipated in the heater element of the convective acceleration sensor (See Page 9, lines 3-6 of the instant specification).

OR,

However, referring to claims 14 and 25, Chen teaches analogous art, wherein the common-mode output voltage is proportional to current flowing through a heater element of a resistive sensor (Col. 1, lines 29-31; Col. 7, lines 1-10 of '775), such as thermocouples, and therefore, the power dissipated in the resistive sensor because Ohm's law teaches $P = R*(I^2)$.

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to combine teachings of AAPA or Chen with Leung or Hosoi.

One of ordinary skill in the art would have been motivated to combine AAPA with Leung or Hosoi because AAPA teaches that it is commonly known in the art that the common-mode output voltage is proportional to power dissipated in the heater element of the convective acceleration sensor (See Page 9, lines 3-6 of the instant specification).

One of ordinary skill in the art would have been motivated to combine Chen with Leung or Hosoi because Chen teaches a low cost signal conditioning circuit for converting a signal having a low amplitude, floating, wide bandwidth characteristics with a high common mode noise to a relatively large, low distortion, ground reference output signal with full-range bi-directional common mode rejection capability (Col. 1, lines 7-11 of '775). Furthermore, it is commonly known in the art that the common-mode output voltage is proportional to power dissipated in the heater element of the convective acceleration sensor (See Page 9, lines 3-6 of the instant specification).

Allowable Subject Matter

10. Claims 2-7, 16-19, and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents or publications are cited to further show the state of the art with respect to converting a differential output voltage to single-ended output voltage with common-mode feedback.

U.S. Pat. No. 6,281,751 to Maulik.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean P. Shechtman whose telephone number is (703) 305-7798. The examiner can normally be reached on Monday-Friday from 9:30am to 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard, can be reached on (703) 308-0538. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9600.

SPS

Sean P. Shechtman

February 19, 2004

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100